In re Patent Application of:
GARNIER ET AL.
Serial No. **09/499,060**
Filing Date: **February 4, 2000**

In the Claims:

Claims 1-8 (Cancelled).

9. (Previously Presented) An integrated circuit voltage ramp generator produced using CMOS technology and comprising:

a capacitance; and

a CMOS charging circuit connected to said capacitance and comprising

a current generator having a first resistance, and

a circuit connected to said current generator and to said capacitance, said circuit having a second resistance and enabling a capacitance charging current to be proportional to a square of a ratio of the second resistance and the first resistance.

10. (Previously Presented) A voltage ramp generator according to Claim 9, wherein said CMOS charging circuit further comprises a degenerate current mirror circuit.

11. (Previously Presented) A voltage ramp generator according to Claim 10, wherein said degenerate current mirror circuit comprises:

a first MOS transistor having a channel of a first conductivity type comprising a gate, a drain and a source, the drain and the gate being connected to said current generator, and the source being connected to said second resistance; and

a second MOS transistor having a channel of the

first conductivity type comprising a gate, a drain and a source, the gate being connected to the gate of said first MOS transistor, the source being connected to a supply voltage, and the drain being connected to said capacitance.

12. (Previously Presented) A voltage ramp generator according to Claim 11, wherein each of said first and second MOS transistors comprises a P-channel MOS transistor.

13. (Previously Presented) A voltage ramp generator according to Claim 9, wherein said capacitance comprises a gate capacitance of a MOS transistor.

14. (Previously Presented) A voltage ramp generator according to Claim 9, wherein current generated by said CMOS current generator is based upon the equation:

$$Ig2 = K2 \times \frac{Vg2}{Rg2}$$

where Ig2 is the current, K2 is a proportionality coefficient, Rg2 is the first resistance, and Vg2 is a reference voltage proportional to the quantity $k\frac{T}{q}$, where k is the Boltzmann constant, T is absolute temperature, and q is the charge of an electron.

15. (Previously Presented) An integrated circuit voltage ramp generator produced using CMOS technology and comprising:

a capacitance; and

a CMOS charging circuit connected to said

capacitance and comprising

a current generator having a first resistance, and

a degenerate current mirror circuit connected to said current generator and to said capacitance, said degenerate current mirror circuit having a second resistance for generating a capacitance charging current that is proportional to a square of a ratio of the second resistance and the first resistance.

16. (Previously Presented) A voltage ramp generator according to Claim 15, wherein said current generator has a first resistance, and said degenerate current mirror circuit has a second resistance such that the capacitance charging current is proportional to a square of a ratio of the second resistance and the first resistance.

17. (Previously Presented) A voltage ramp generator according to Claim 15, wherein said degenerate current mirror circuit comprises:

a first MOS transistor having a channel of a first conductivity type comprising a gate, a drain and a source, the drain and the gate being connected to said current generator, and the source being connected to said second resistance; and

a second MOS transistor having a channel of the first conductivity type comprising a gate, a drain and a source, the gate being connected to the gate of said first MOS transistor, the source being connected to a supply voltage, and the drain being connected to said capacitance.

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18. (Previously Presented) A voltage ramp generator according to Claim 17, wherein each of said first and second MOS transistors comprises a P-channel MOS transistor.

19. (Previously Presented) A voltage ramp generator according to Claim 15, wherein said capacitance comprises a gate capacitance of a MOS transistor.

20. (Previously Presented) A voltage ramp generator according to Claim 15, wherein current generated by said current generator is based upon the equation:

$$Ig2 = K2 \times \frac{Vg2}{Rg2}$$

where Ig2 is the current, K2 is a proportionality coefficient, Rg2 is the first resistance, and Vg2 is a reference voltage proportional to the quantity $k\frac{T}{q}$, where k is the Boltzmann constant, T is absolute temperature, and q is the charge of an electron.

21. (Currently Amended) An integrated circuit current ramp generator produced using CMOS technology and comprising:

a voltage ramp generator comprising

a capacitance, and

a CMOS charging circuit connected to said capacitance and comprising

a current generator having a first resistance, and

a circuit connected to said current generator and to said capacitance, said circuit having a second resistance and enabling a capacitance charging current to be proportional to a square of a ratio of the second resistance and the first resistance; and

a conversion circuit connected to said voltage ramp generator for generating a current ~~ramp.~~ ramp and comprising an implanted resistance having a positive temperature coefficient.

Claim 22 (Cancelled).

Claim 23 (Cancelled).

24. (Previously Presented) An integrated circuit current ramp generator according to Claim 21, wherein said CMOS charging circuit further comprises a degenerate current mirror circuit.

25. (Previously Presented) A current ramp generator according to Claim 24, wherein said degenerate current mirror circuit comprises:

a first MOS transistor having a channel of a first conductivity type comprising a gate, a drain and a source, the drain and the gate being connected to said current generator, and the source being connected to said second resistance; and

a second MOS transistor having a channel of the first conductivity type comprising a gate, a drain and a source, the gate being connected to the gate of said first MOS

transistor, the source being connected to a supply voltage, and the drain being connected to said capacitance.

26. (Previously Presented) A current ramp generator according to Claim 25, wherein each of said first and second MOS transistors comprises a P-channel MOS transistor.

27. (Previously Presented) A current ramp generator according to Claim 21, wherein said capacitance comprises a gate capacitance of a MOS transistor.

28. (Previously Presented) A current ramp generator according to Claim 21, wherein current generated by said current generator is based upon the equation:

$$Ig2 = K2 \times \frac{Vg2}{Rg2}$$

where Ig2 is the current, K2 is a proportionality coefficient, Rg2 is the first resistance, and Vg2 is a reference voltage proportional to the quantity $k\frac{T}{q}$, where k is the Boltzmann constant, T is absolute temperature, and q is the charge of an electron.

29. (Currently Amended) An integrated circuit current ramp generator produced using CMOS technology and comprising:

a voltage ramp generator comprising

a capacitance having a first resistance, and

a CMOS charging circuit connected to said capacitance and comprising

a current generator, and

a degenerate current mirror circuit connected to said current generator and to said capacitance, said degenerate current mirror circuit having a second resistance for generating a capacitance charging current that is proportional to a square of a ratio of the second resistance and the first resistance; and

a third resistance connected to said voltage ramp generator for generating a current ~~ramp.~~ ramp, said third resistance comprising an implanted resistance having a positive temperature coefficient.

30. (Previously Presented) A current ramp generator according to Claim 29, wherein said current generator has a first resistance, and said degenerate current mirror circuit has a second resistance such that the capacitance charging current is proportional to a square of a ratio of the second resistance and the first resistance.

Claim 31 (Cancelled).

32. (Previously Presented) A current ramp generator according to Claim 29, wherein said degenerate current mirror circuit comprises:

a first MOS transistor having a channel of a first conductivity type comprising a gate, a drain and a source, the drain and the gate being connected to said CMOS current generator, and the source being connected to said second resistance; and

a second MOS transistor having a channel of the first conductivity type comprising a gate, a drain and a source, the gate being connected to the gate of said first MOS transistor, the source being connected to a supply voltage, and the drain being connected to said capacitance.

33. (Previously Presented) A current ramp generator according to Claim 32, wherein each of said first and second MOS transistors comprises a P-channel MOS transistor.

34. (Previously Presented) A current ramp generator according to Claim 29, wherein said capacitance comprises a gate capacitance of a MOS transistor.

35. (Previously Presented) A current ramp generator according to Claim 29, wherein current generated by said current generator is based upon the equation:

$$Ig2 = K2 \times \frac{Vg2}{Rg2}$$

where Ig2 is the current, K2 is a proportionality coefficient, Rg2 is the first resistance, and Vg2 is a reference voltage proportional to the quantity $k\frac{T}{q}$, where k is the Boltzmann constant, T is absolute temperature, and q is the charge of an electron.

36. (Previously Presented) A method for generating a ramp voltage comprising:

generating a capacitance charging current using an integrated circuit charging circuit produced using CMOS

technology and comprising a current generator having a first resistance and a circuit connected to the generator, the circuit having a second resistance and enabling the capacitance charging current to be proportional to a square of a ratio of the second resistance and the first resistance; and

charging a capacitance with the capacitance charging current for generating the ramp voltage.

37. (Previously Presented) A method according to Claim 36, wherein the circuit further comprises a degenerate current mirror circuit.

Claims 38-39 (Cancelled).

40. (Previously Presented) A method according to Claim 36, wherein current generated by the current generator is based upon the equation:

$$Ig2 = K2 \times \frac{Vg2}{Rg2}$$

where Ig2 is the current, K2 is a proportionality coefficient, Rg2 is the first resistance, and Vg2 is a reference voltage proportional to the quantity $k\frac{T}{q}$, where k is the Boltzmann constant, T is absolute temperature, and q is the charge of an electron.